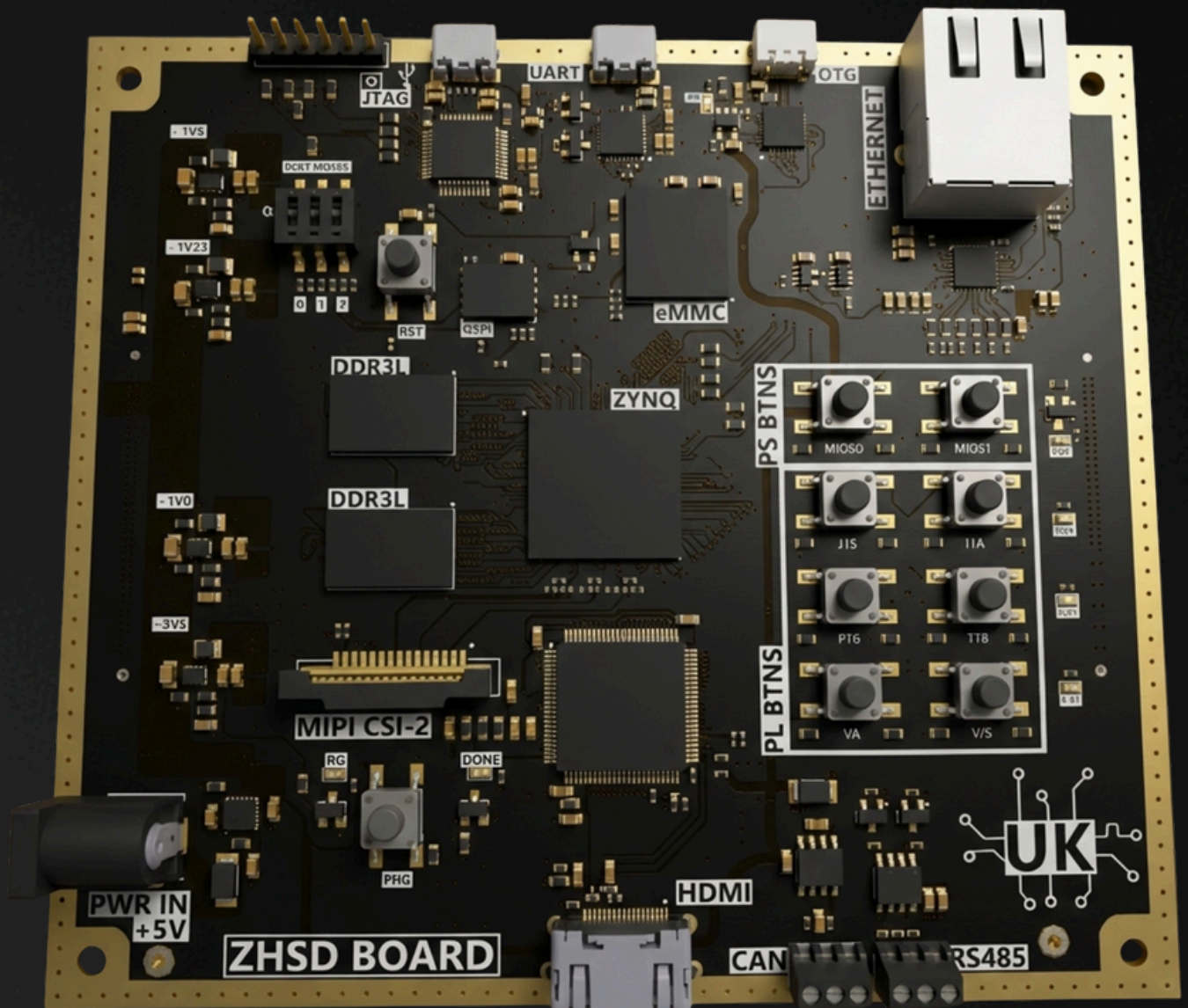
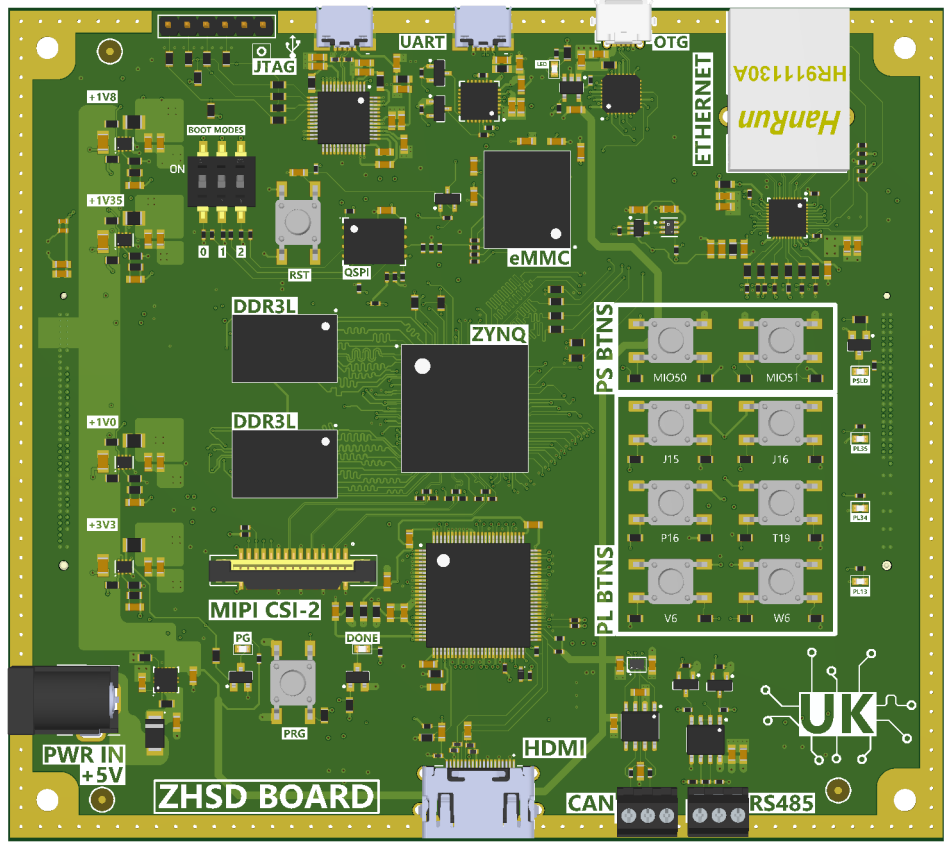


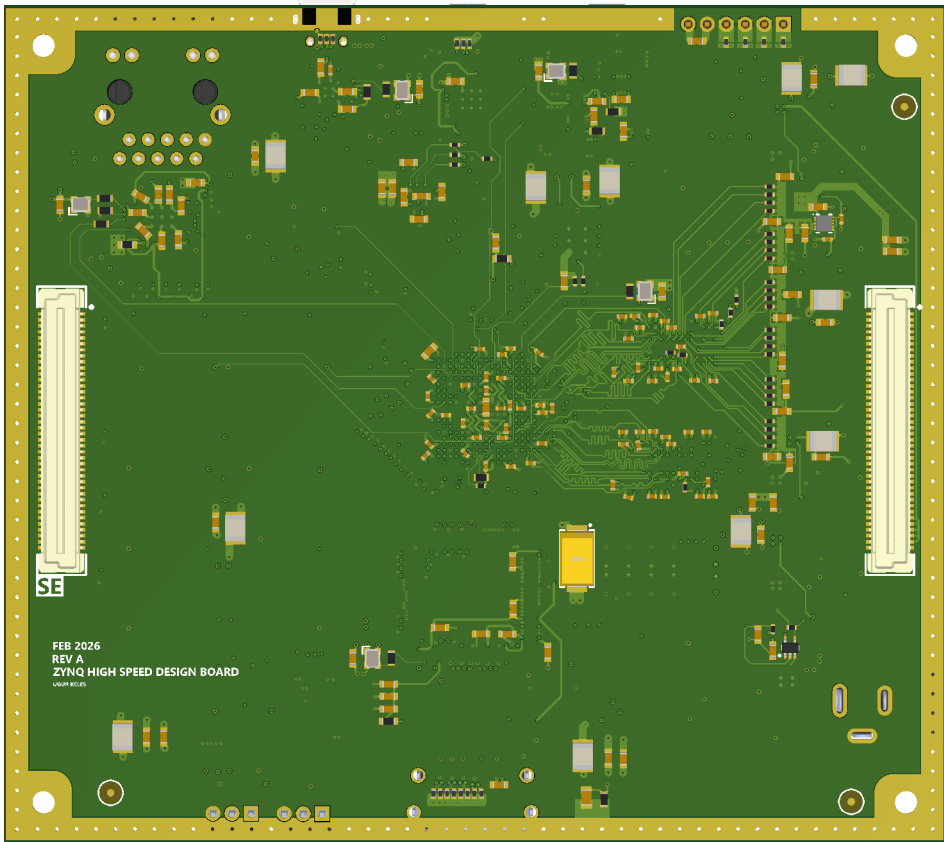
ZYNQ-BASED HIGH SPEED DESIGN



Realistic View



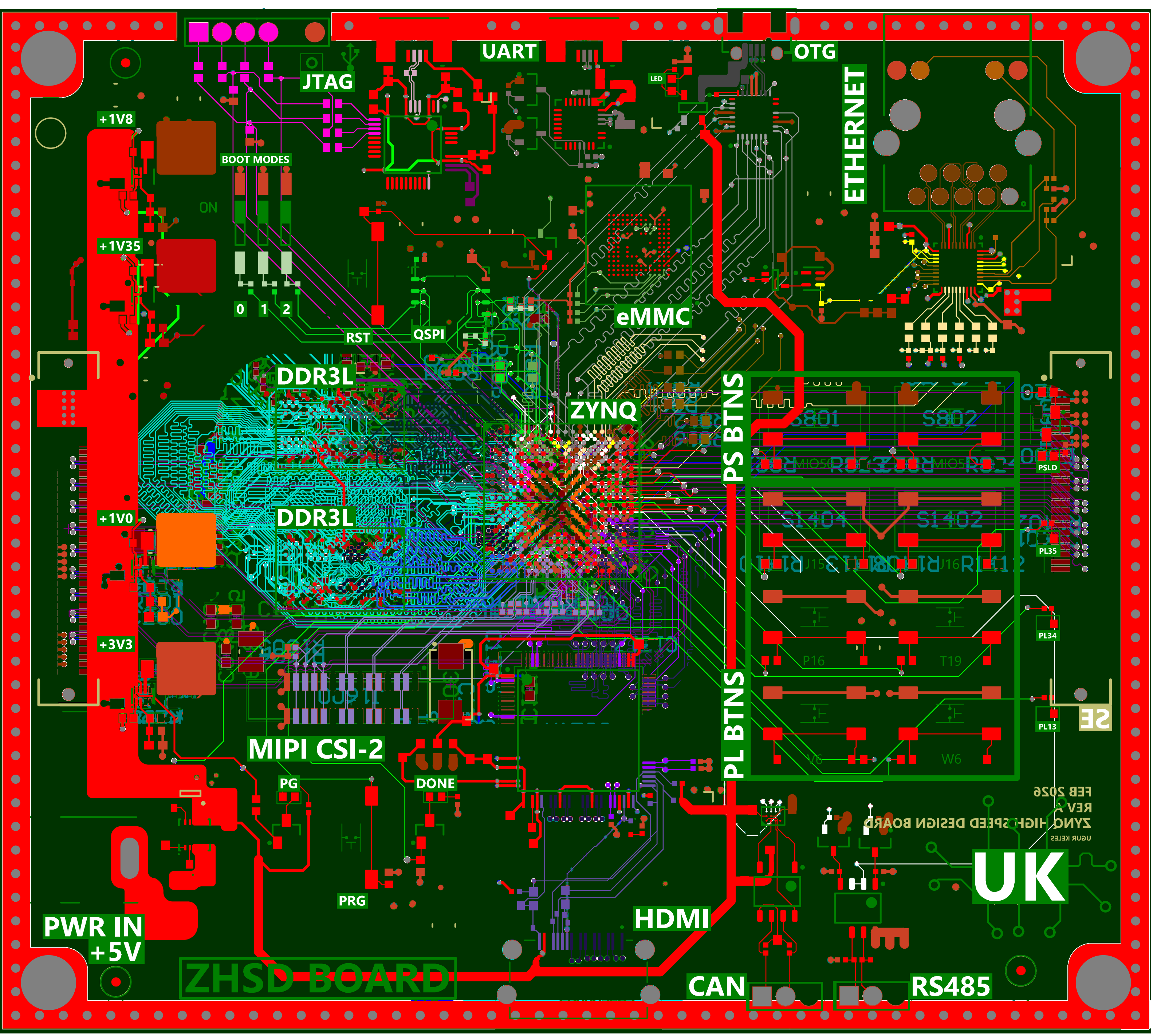
Realistic View



Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask	GTS
Copper	S1 (SIG)	0.04mm		Signal	GTL
Prepreg		0.08mm	PP-008	Dielectric	
CF-004	S2 (GND)	0.02mm		Signal	G1
Core		0.08mm	Core-005	Dielectric	
CF-004	S3 (SIG)	0.02mm		Signal	G2
Prepreg		0.08mm	PP-006	Dielectric	
Prepreg		0.08mm	PP-006	Dielectric	
CF-004	S4 (GND)	0.02mm		Signal	G3
Core		0.08mm	Core-028	Dielectric	
CF-004	S5 (PWR)	0.02mm		Signal	G4
Prepreg		0.21mm	PP-022	Dielectric	
Prepreg		0.22mm	PP-023	Dielectric	
Prepreg		0.21mm	PP-022	Dielectric	
CF-004	S6 (SIG)	0.02mm		Signal	G5
Core		0.08mm	Core-028	Dielectric	
CF-004	S7 (GND)	0.02mm		Signal	G6
Prepreg		0.08mm	PP-006	Dielectric	
Prepreg		0.08mm	PP-006	Dielectric	
CF-004	S8 (SIG)	0.02mm		Signal	G7
Core		0.08mm	Core-005	Dielectric	
CF-004	S9 (GND)	0.02mm		Signal	G8
Prepreg		0.08mm	PP-008	Dielectric	
Copper	S10 (SIG)	0.04mm		Signal	GBL
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1.62mm



UART

OTG

ETHERNET

JTAG

+1V8

BOOT MODES

+1V35

0 1 2

RST

QSPI

eMMC

DDR3L

ZYNQ

PS BTNS

+1V0

DDR3L

+3V3

PL BTNS

MIPI CSI-2

PG

DONE

PWR IN
+5V

HDMI

ZHSD-BOARD

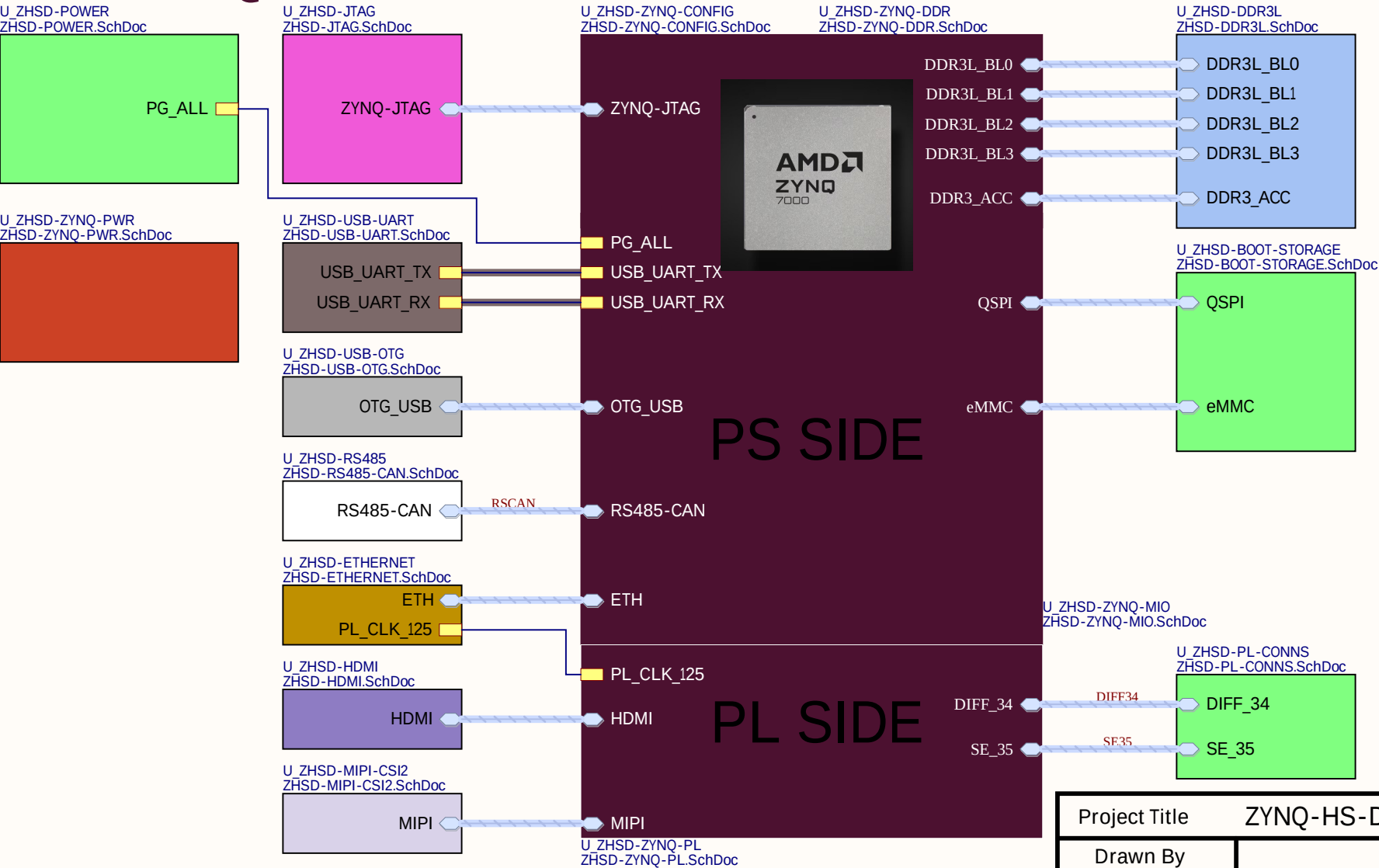
CAN

RS485

UK

ZYNQ HIGH-SPEED DESIGN BOARD
NGUR KETES
REV A
FEB 2026

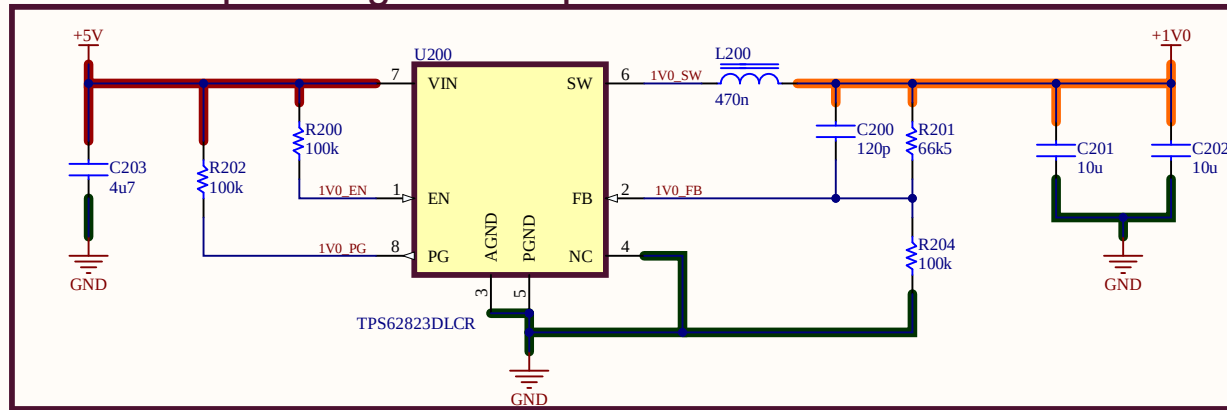
ZYNQ-7000 HIGH SPEED DESIGN



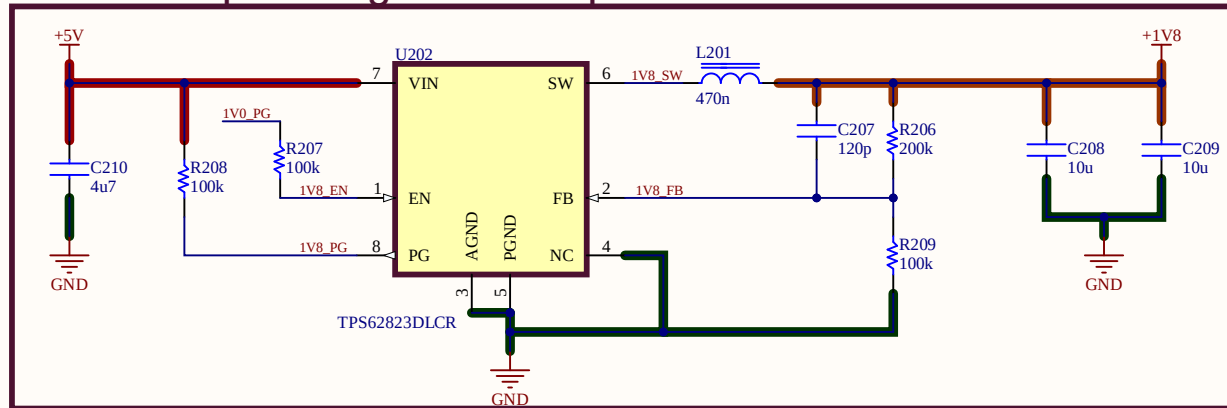
Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By		Sheet Name	
Uğur KELEŞ		ZHSD-Block.SchDoc	
Date	9.02.2026	Sheet	1 / 17
		Sheet Size A4	

ZHSD POWER SYSTEM

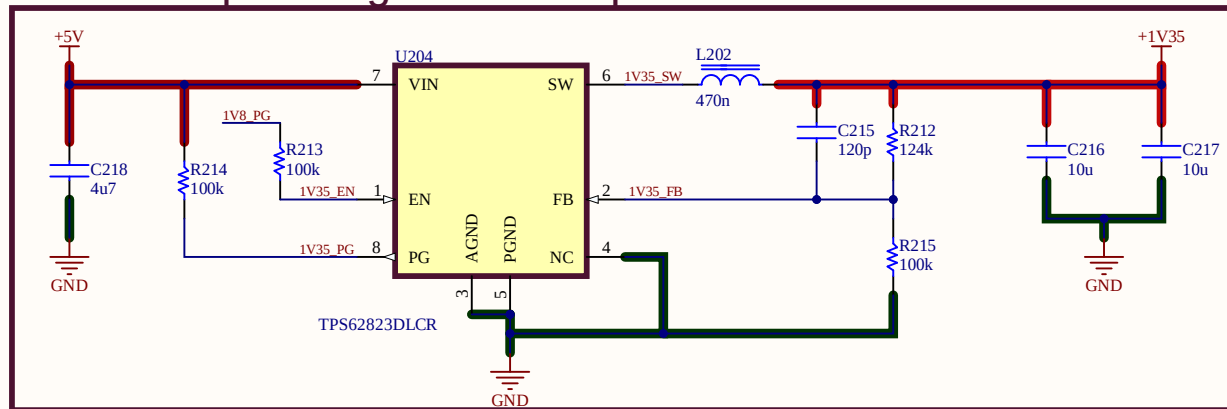
Power Sequencing - 1V Output



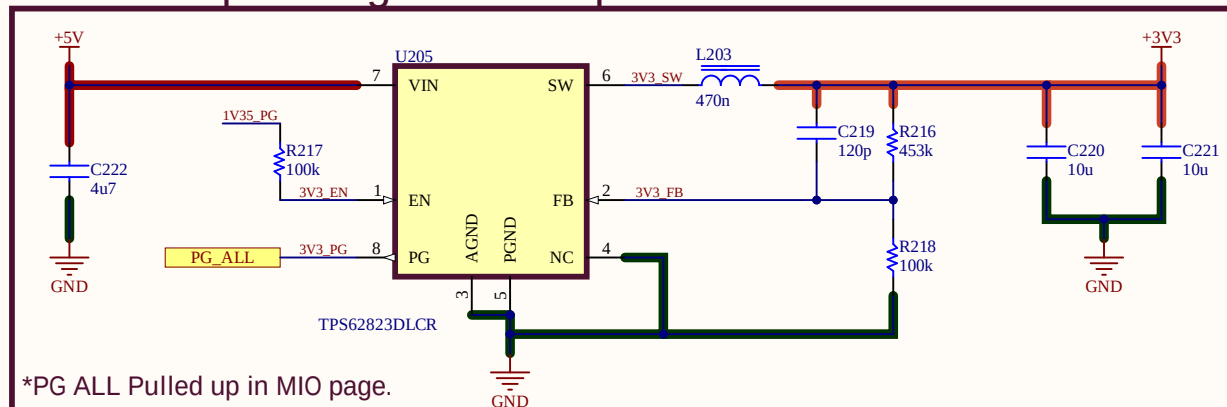
Power Sequencing - 1V8 Output



Power Sequencing - 1V35 Output

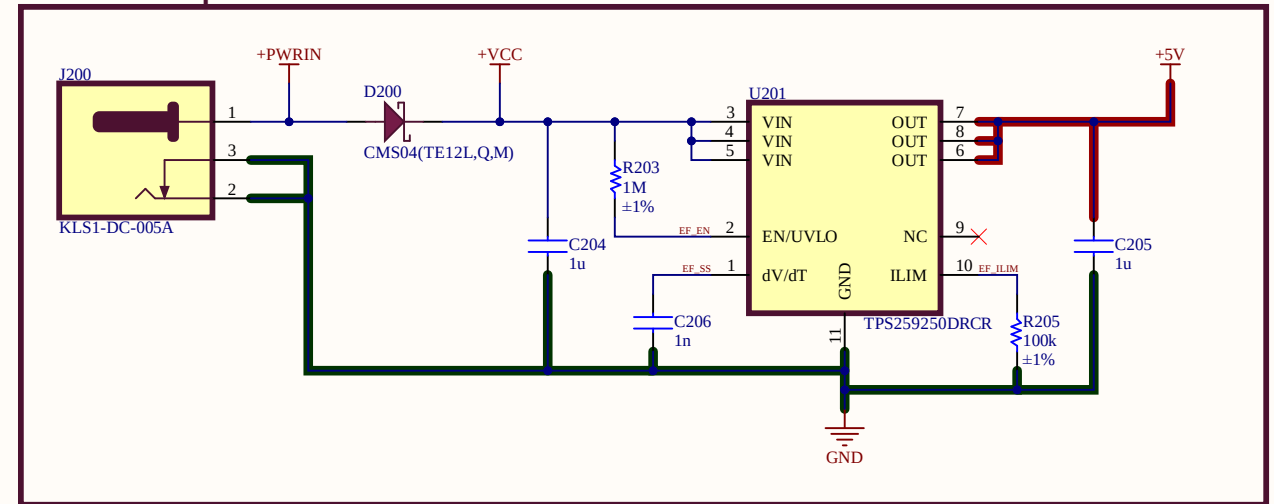


Power Sequencing - 3V3 Output

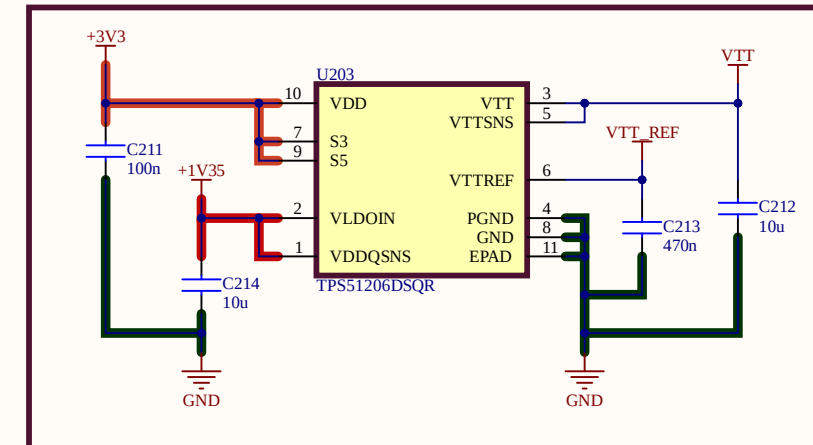


*PG ALL Pulled up in MIO page.

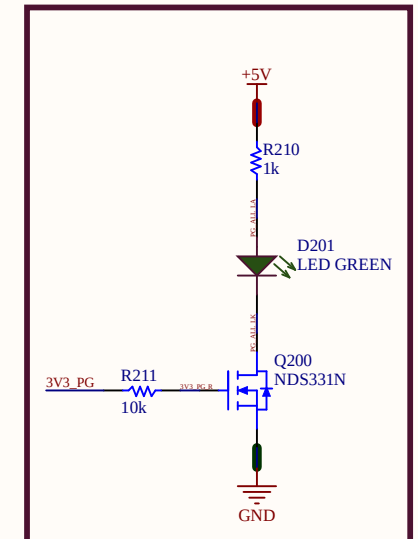
Power Input & EFuse



VTT



PG Led



Power Sequence

*Zynq-7000 SoC DC and AC Switching Characteristics DS187

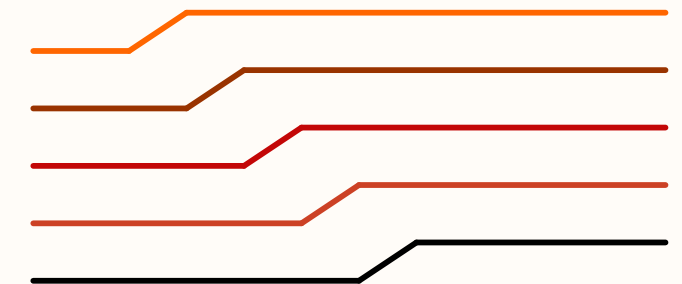
+1V0 VCCPINT, VCCINT, VCCBRAM

+1V8 VCCPAUX, VCCPLL, VCCO_MIO1, VCCAUX

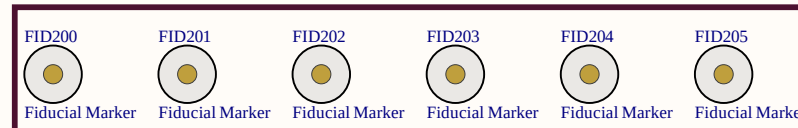
+1V35 VCCO_DDR

+3V3 VCCO_MIO0, VCCO(PL Banks)

+VTT DDR3L Reference Voltage



Fiducials

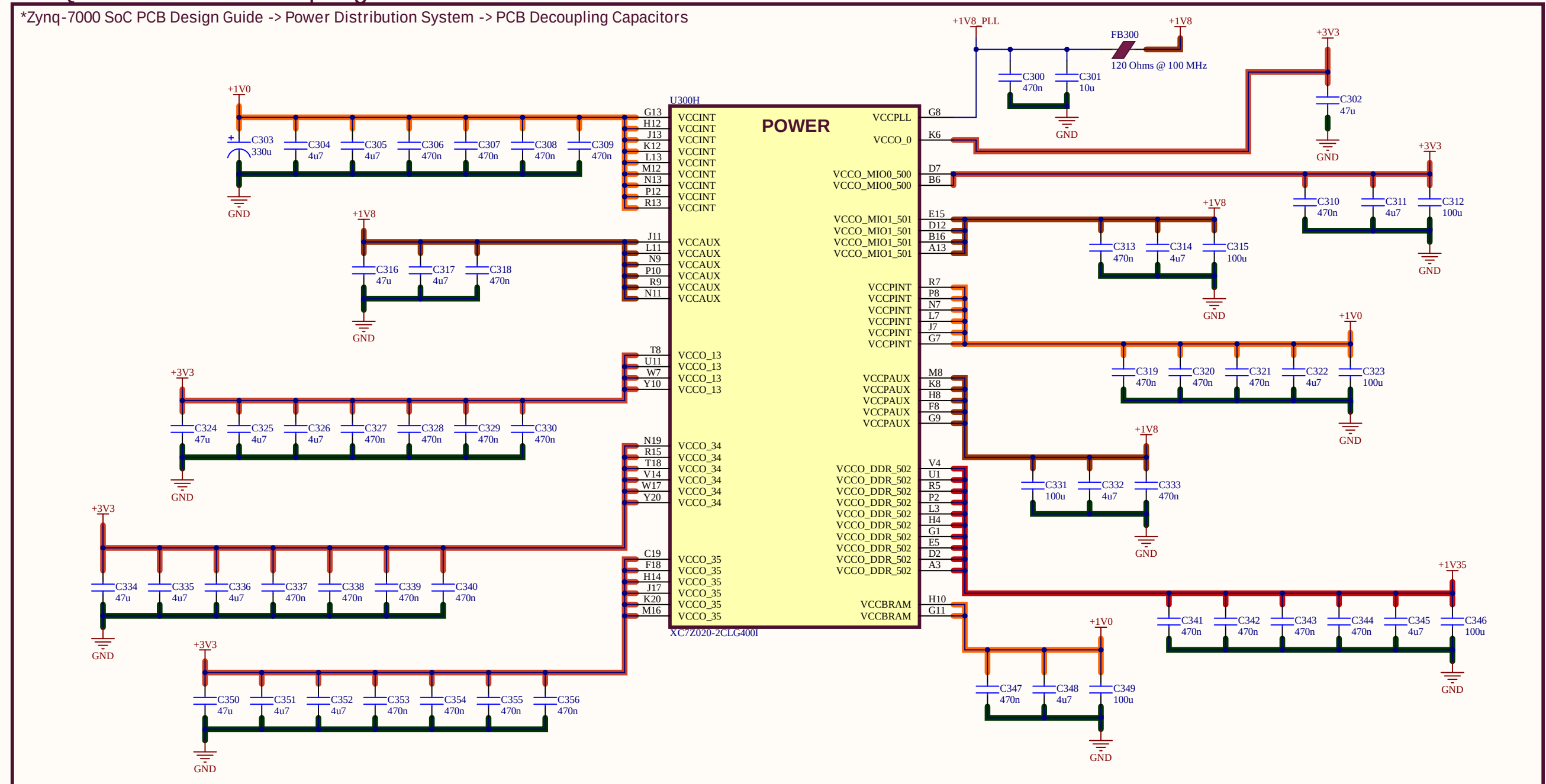


Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By		Sheet Name	
Uğur KELEŞ		ZHSD-POWER.SchDoc	
Date	8.02.2026	Sheet	2 / 17
		Sheet Size A3	

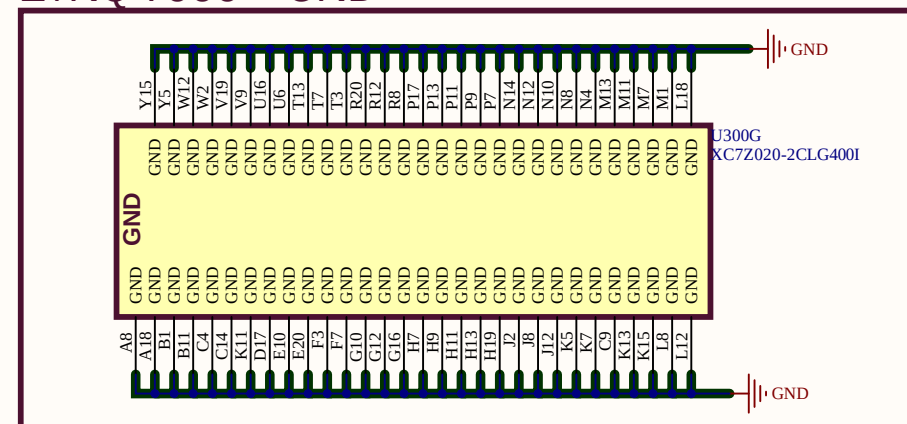
ZHSD ZYNQ POWER DECOUPLING

ZYNQ 7000 Power Decoupling

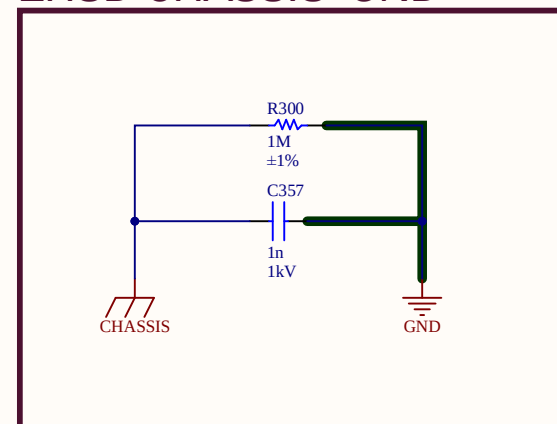
*Zynq-7000 SoC PCB Design Guide -> Power Distribution System -> PCB Decoupling Capacitors



ZYNQ 7000 - GND



ZHSD CHASSIS-GND

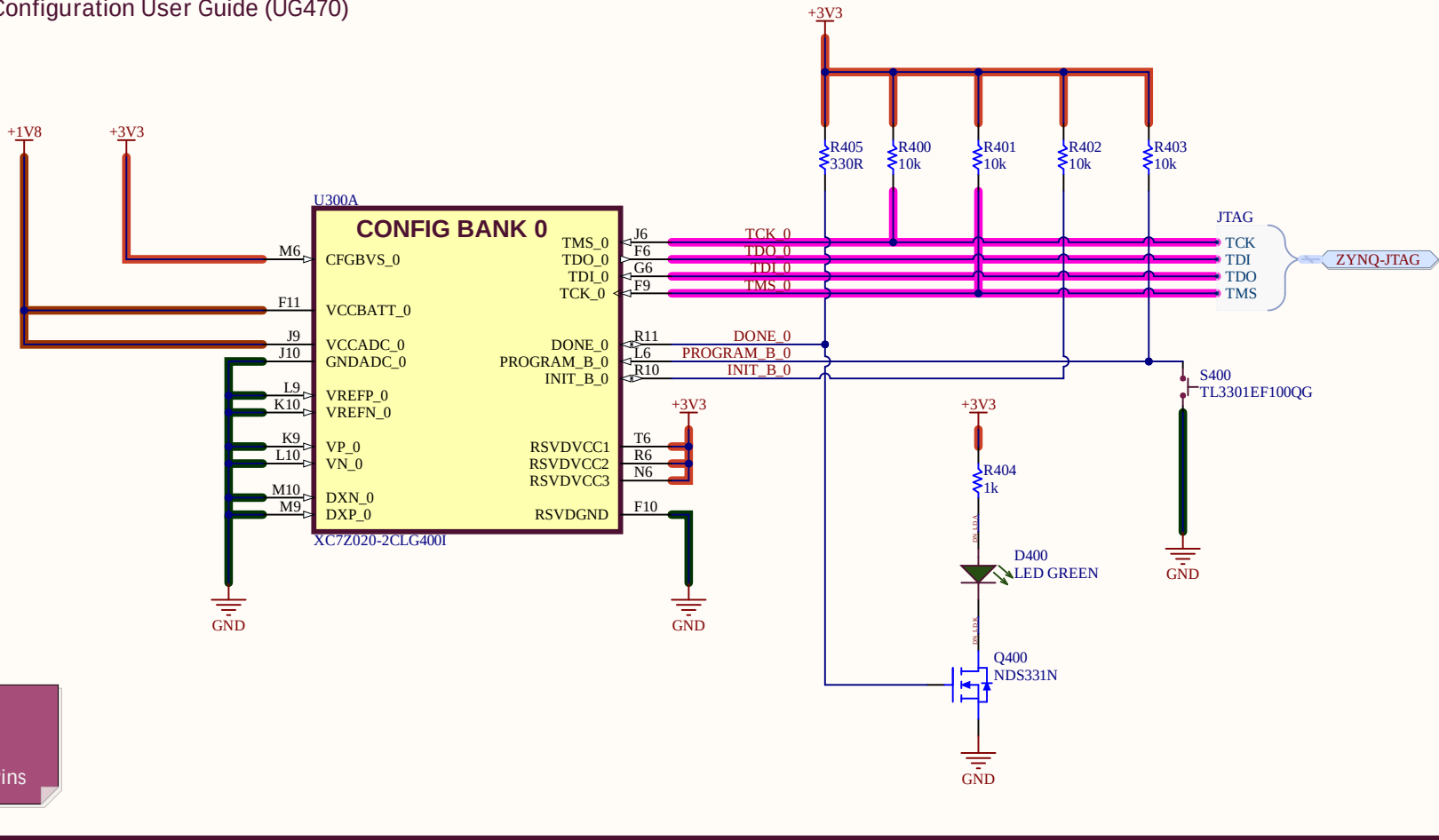


Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By Uğur KELEŞ		Sheet Name ZHSD-ZYNQ-PWR.SchDoc	
Date	8.02.2026	Sheet	3 / 17
		Sheet Size A3	

ZHSD ZYNQ CONFIG

ZYNQ-7000 Config Bank 0

*7 Series FPGAs Configuration User Guide (UG470)



UG480 p9 xADC
UG933 p68 DXP/N
UG865 p13 RSVD
UG470 p20 Other Pins

Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By		Sheet Name	
Uğur KELEŞ		ZHSD-ZYNQ-CONFIG.SchDoc	
Date	8.02.2026	Sheet	4 / 17
		Sheet Size A4	

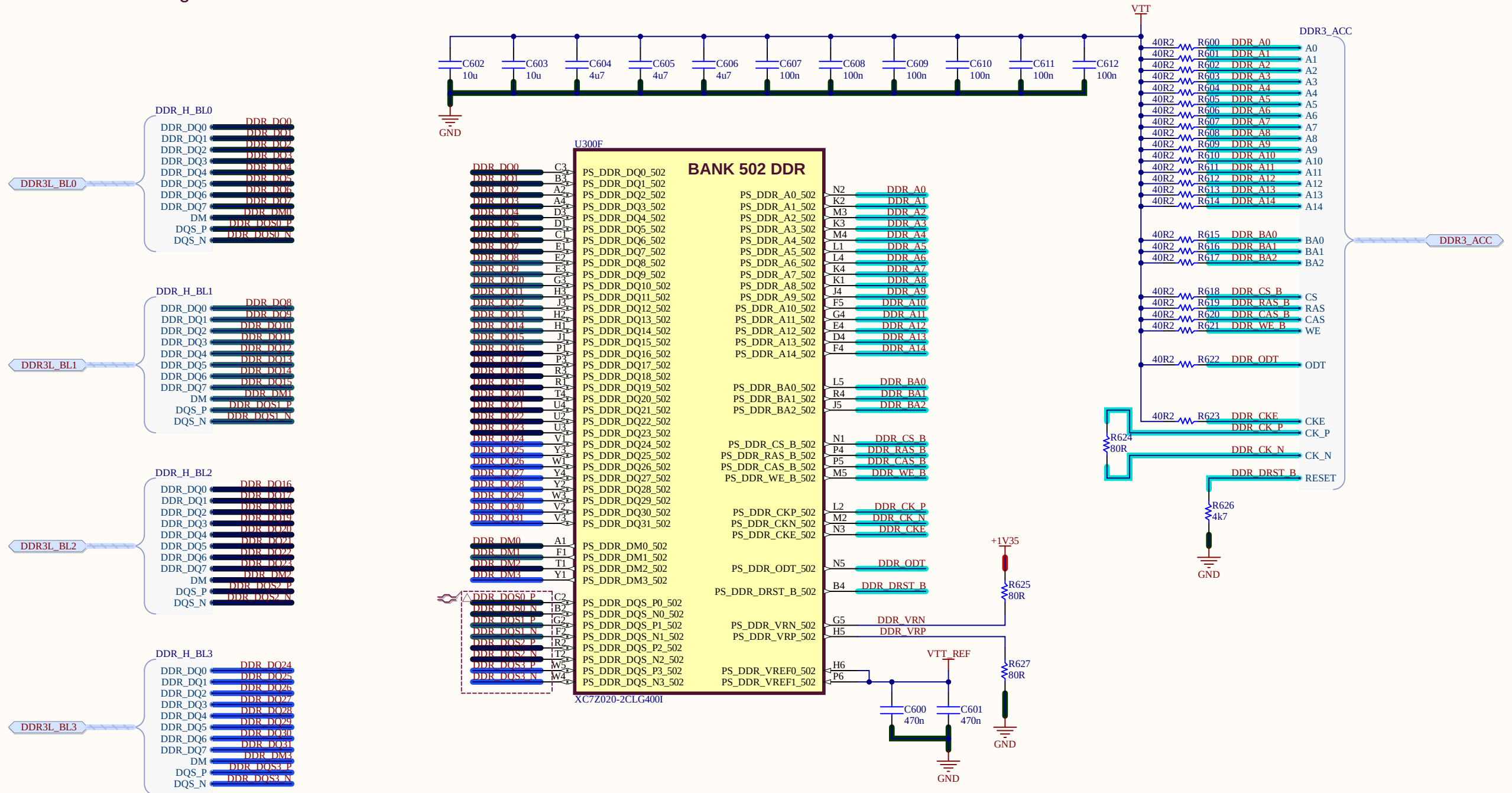
USB-JTAG

Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By Uğur KELEŞ		Sheet Name ZHSD-JTAG.SchDoc	
Date	10.02.2026	Sheet	5 / 17
		Sheet Size A4	

ZHSD ZYNQ DDR3L

ZYNQ-7000 DDR BANK 502

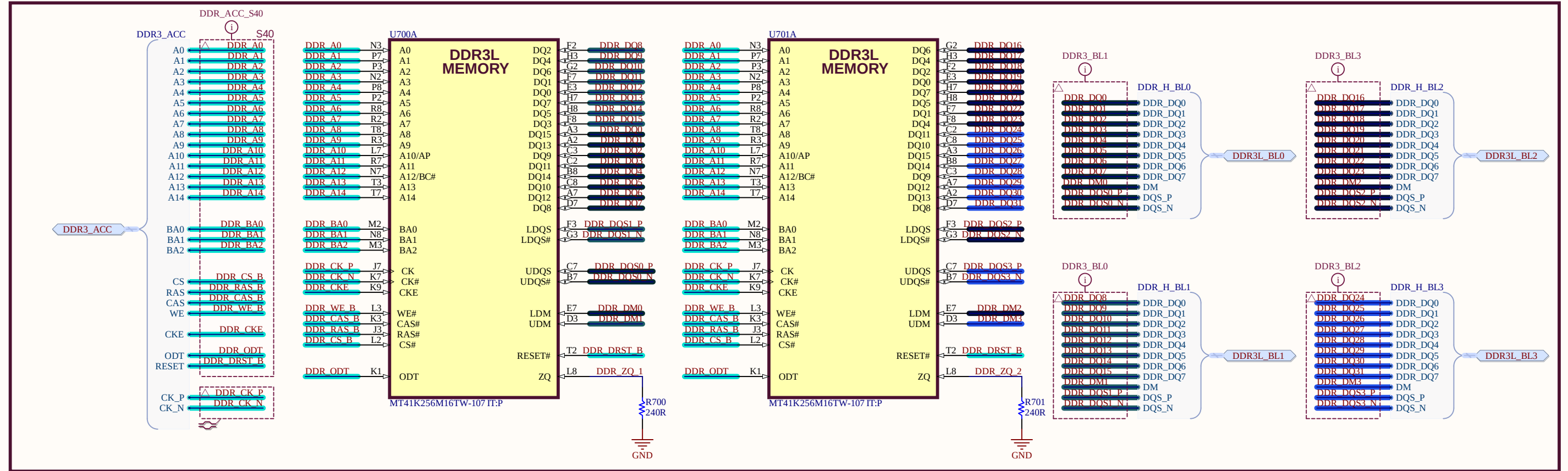
*Zynq-7000 SoC PCB Design Guide UG933



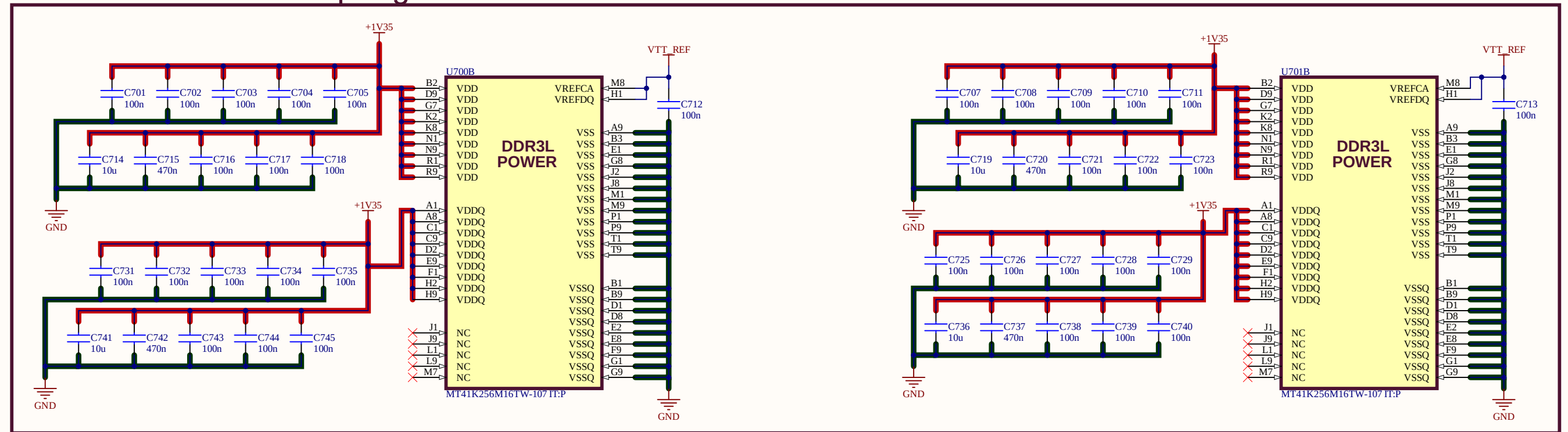
Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By		Sheet Name	
Uğur KELEŞ		ZHSD-ZYNQ-DDR.SchDoc	
Date	9.02.2026	Sheet	6 / 17
		Sheet Size A3	

DDR3L IC

ZHSD DDR3L 1GB



DDR3 IC Power Decoupling

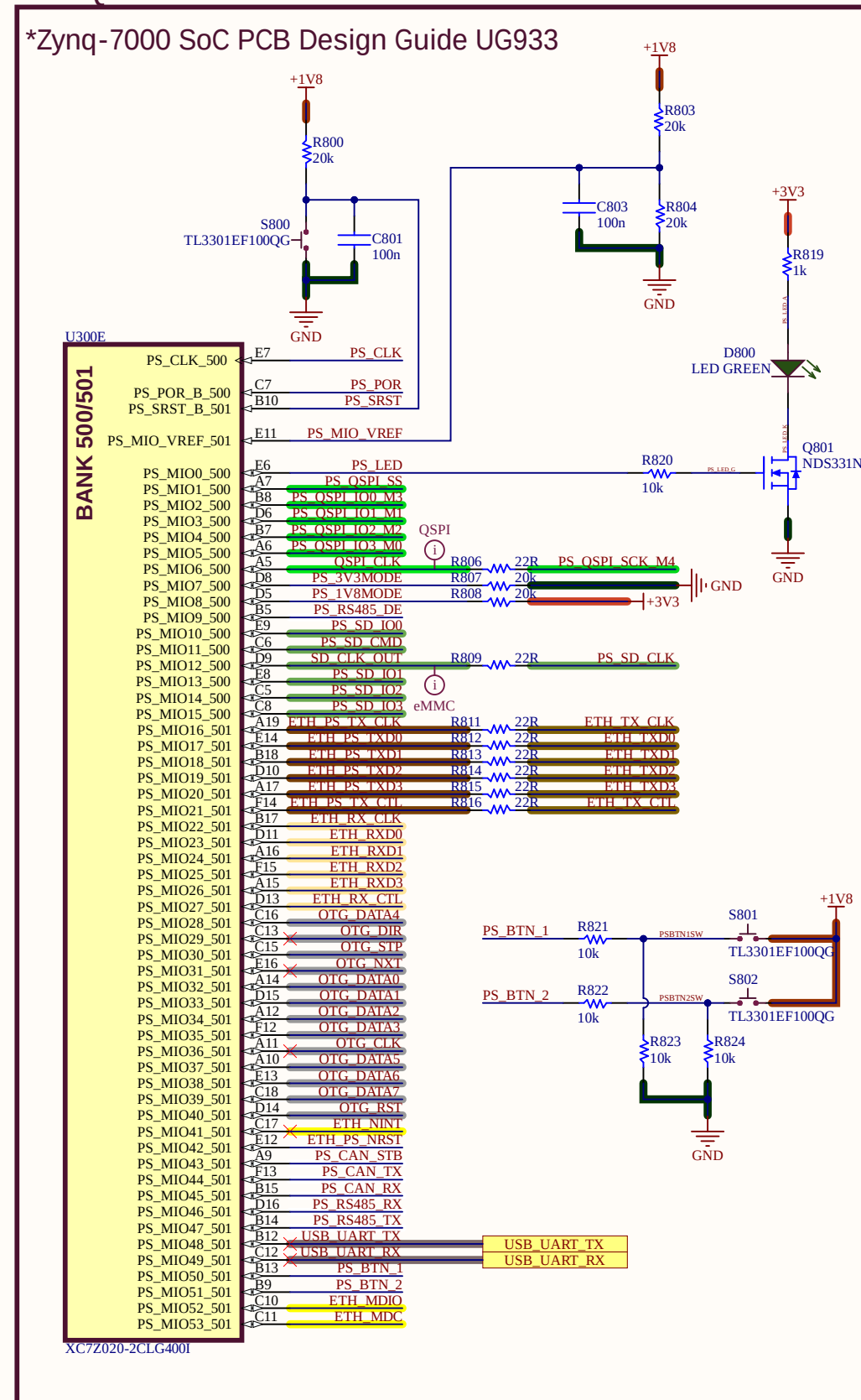


Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By		Sheet Name	
Uğur KELEŞ		ZHSD-DDR3L.SchDoc	
Date	10.02.2026	Sheet	7 / 17
		Sheet Size A3	

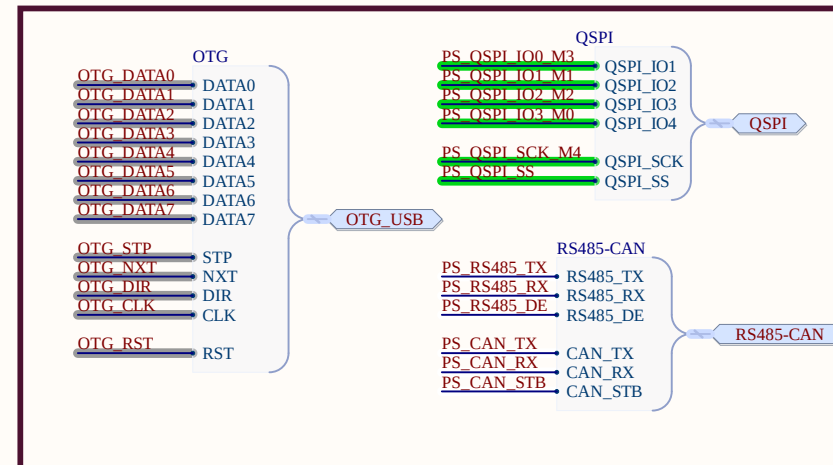
ZHSD ZYNQ PS MIO

ZYNQ-7000 MIO BANK 500/501

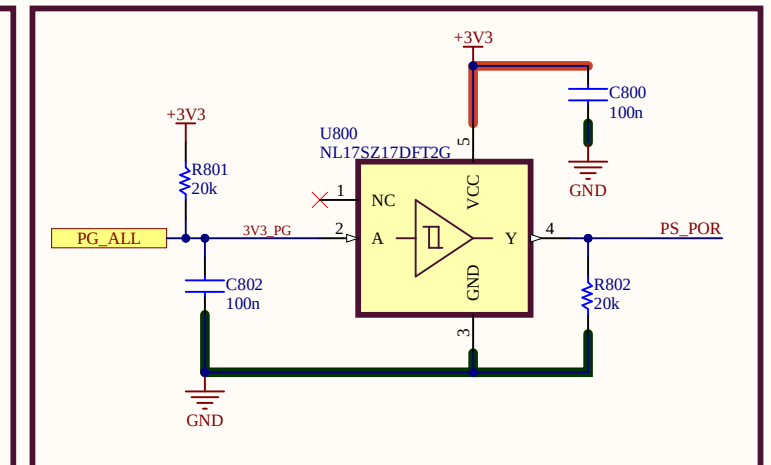
*Zynq-7000 SoC PCB Design Guide UG933



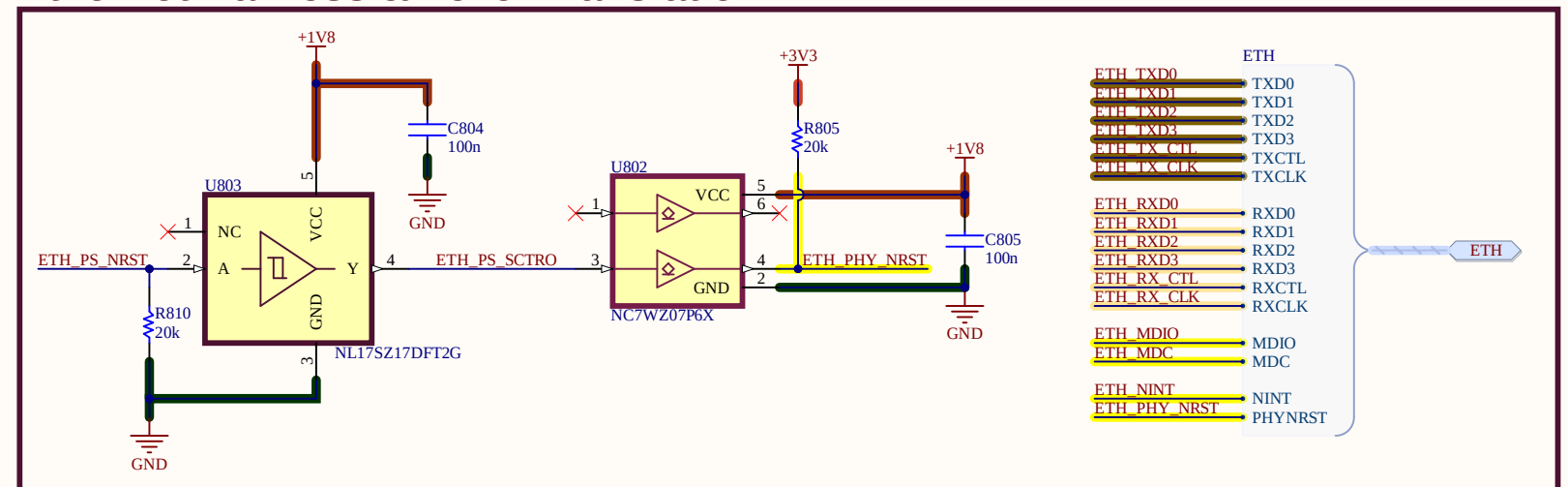
Other Harnesses



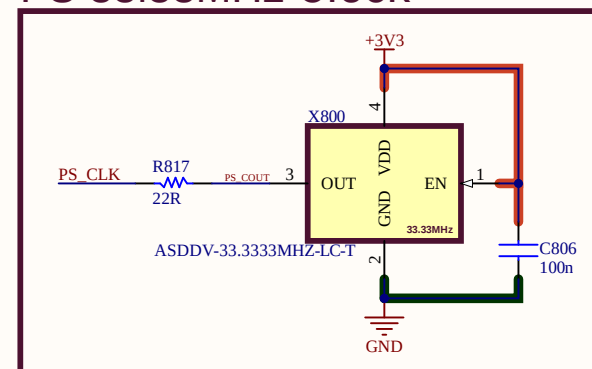
PS Power-On-Reset



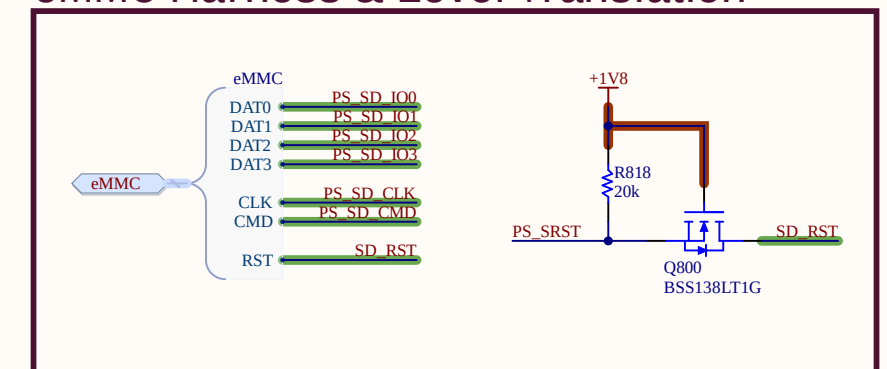
Ethernet Harness & Level Translation



PS 33.33MHz Clock



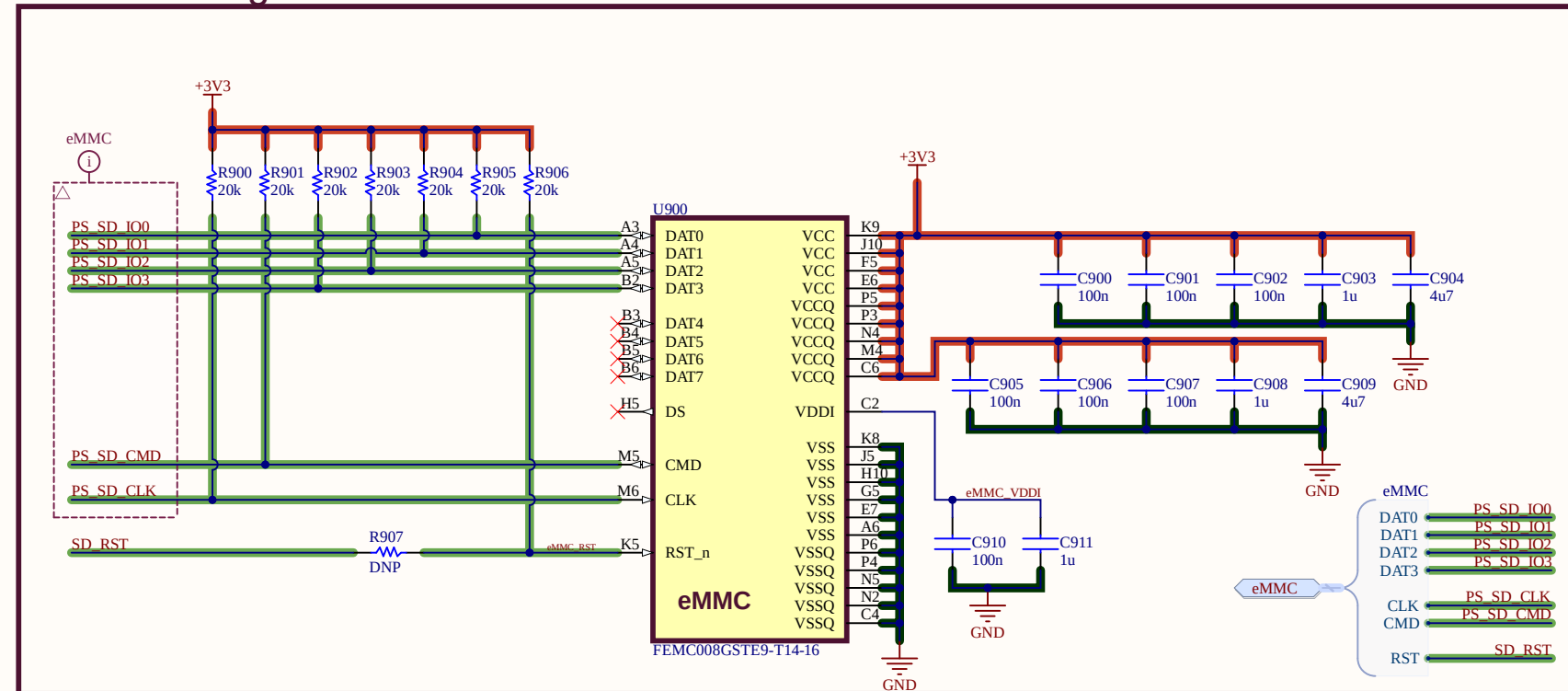
eMMC Harness & Level Translation



Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By Uğur KELEŞ		Sheet Name ZHSD-ZYNQ-MIO.SchDoc	
Date	8.02.2026	Sheet	8 / 17
		Sheet Size A3	

ZHSD BOOTING & STORAGE

eMMC Storage



ZYNQ Boot Modes Reference

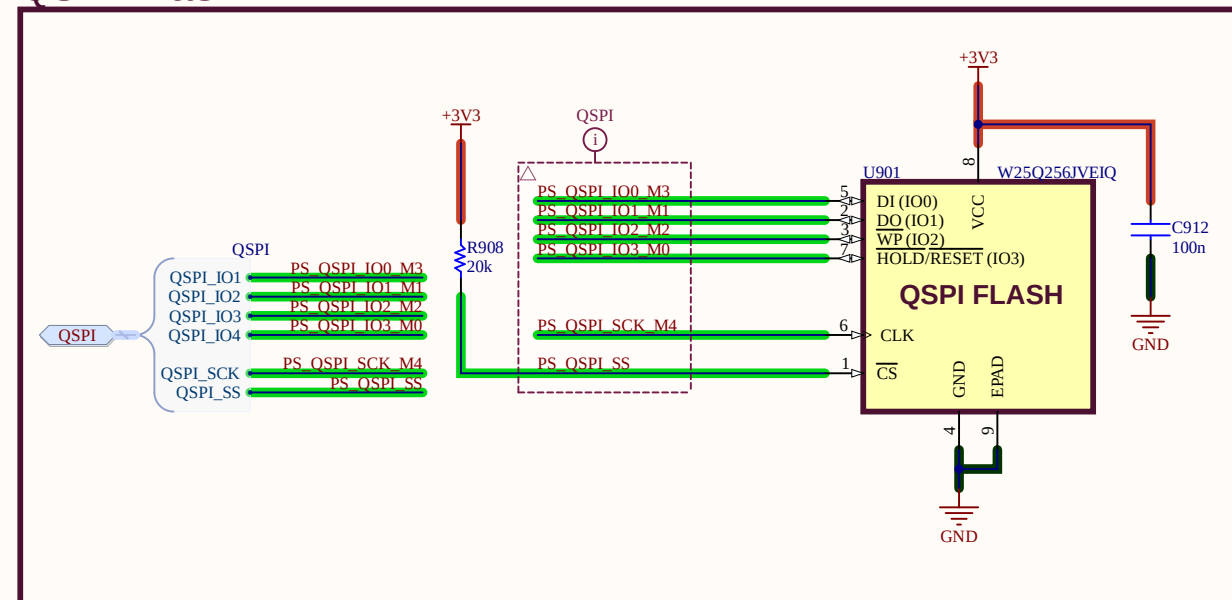
Table 6-4: Boot Mode MIO Strapping Pins

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common ⁽¹⁾				0	0	0	JTAG Chain Routing ⁽²⁾ 0: Cascade mode 1: Independent mode
NOR Boot ⁽³⁾				0	0	1	
NAND				0	1	0	
Quad-SPI ⁽³⁾				1	0	0	
SD Card				1	1	0	
Mode for all 3 PLLs							
PLL Enabled			0	Hardware waits for PLL to lock, then executes BootROM.			
PLL Bypassed			1	Allows for a wide PS_CLK frequency range.			
MIO Bank Voltage ⁽⁴⁾							
	Bank 1	Bank 0	Voltage Bank 0 includes MIO pins 0 thru 15. Voltage Bank 1 includes MIO pins 16 thru 53.				
2.5 V, 3.3 V	0	0					
1.8 V	1	1					

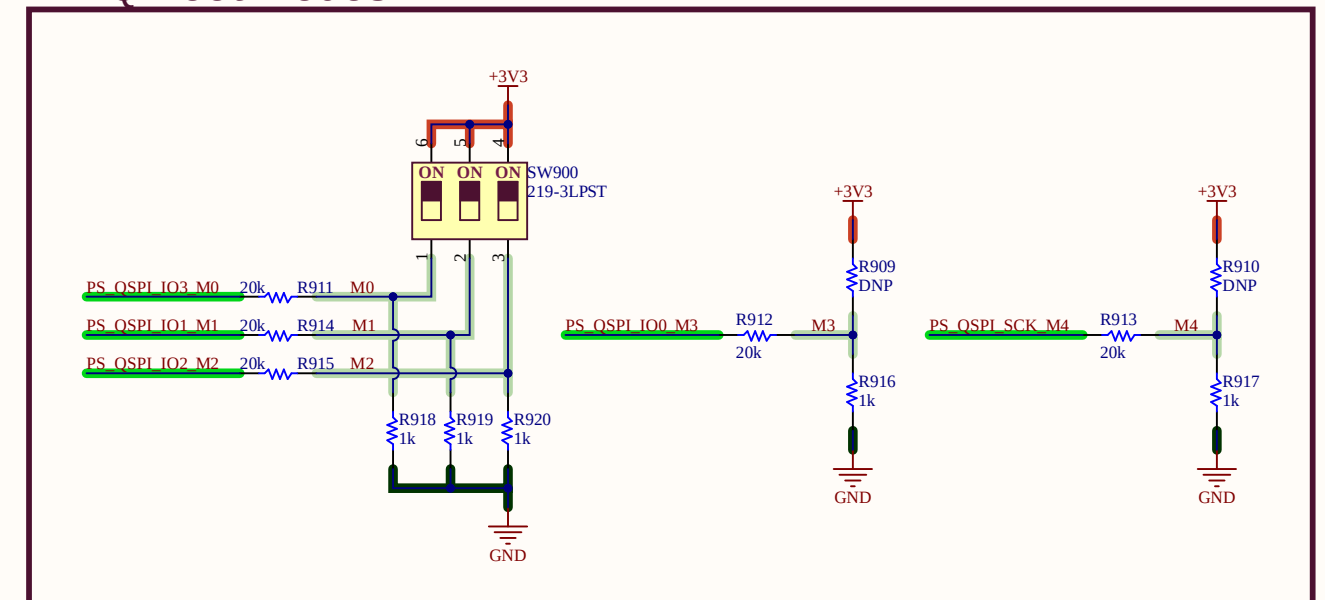
Notes:

1. JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.
2. For secure mode, JTAG is not enabled and MIO[2] is ignored.
3. The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure)
4. Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.

QSPI Flash



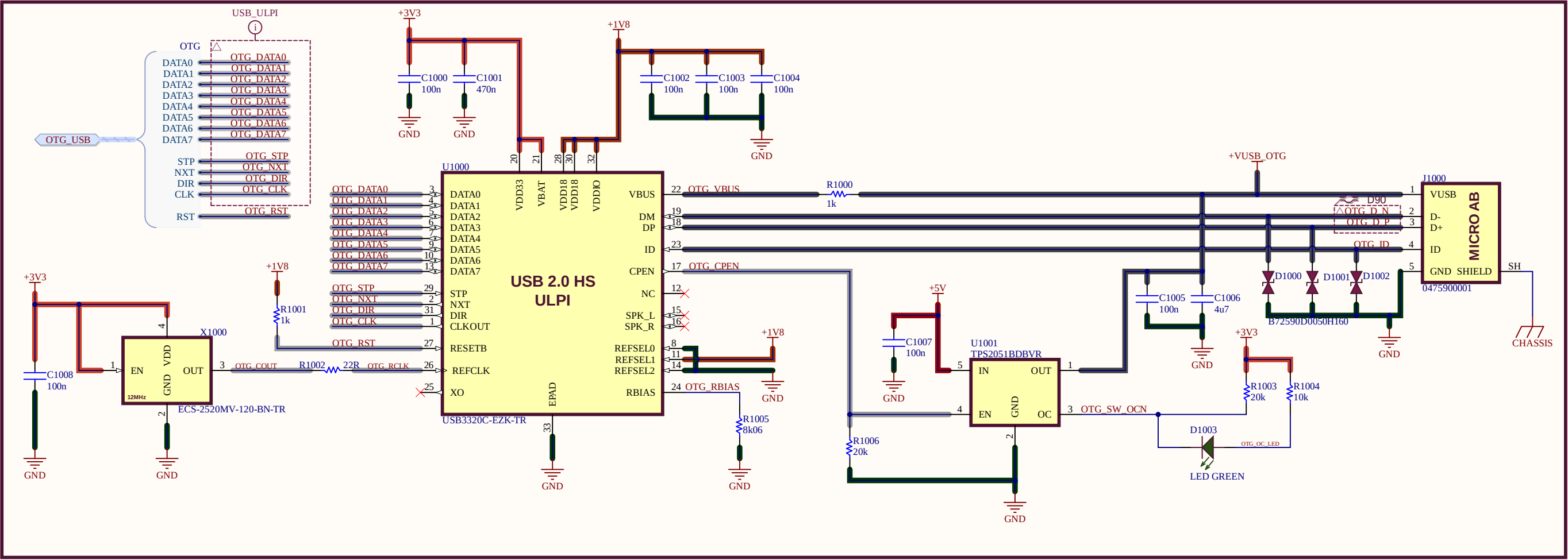
ZYNQ Boot Modes



Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By		Sheet Name	
Uğur KELEŞ		ZHSD-BOOT-STORAGE.SchDoc	
Date	7.02.2026	Sheet	9 / 17
		Sheet Size A3	

ZHSD USB OTG 2.0 ULPI

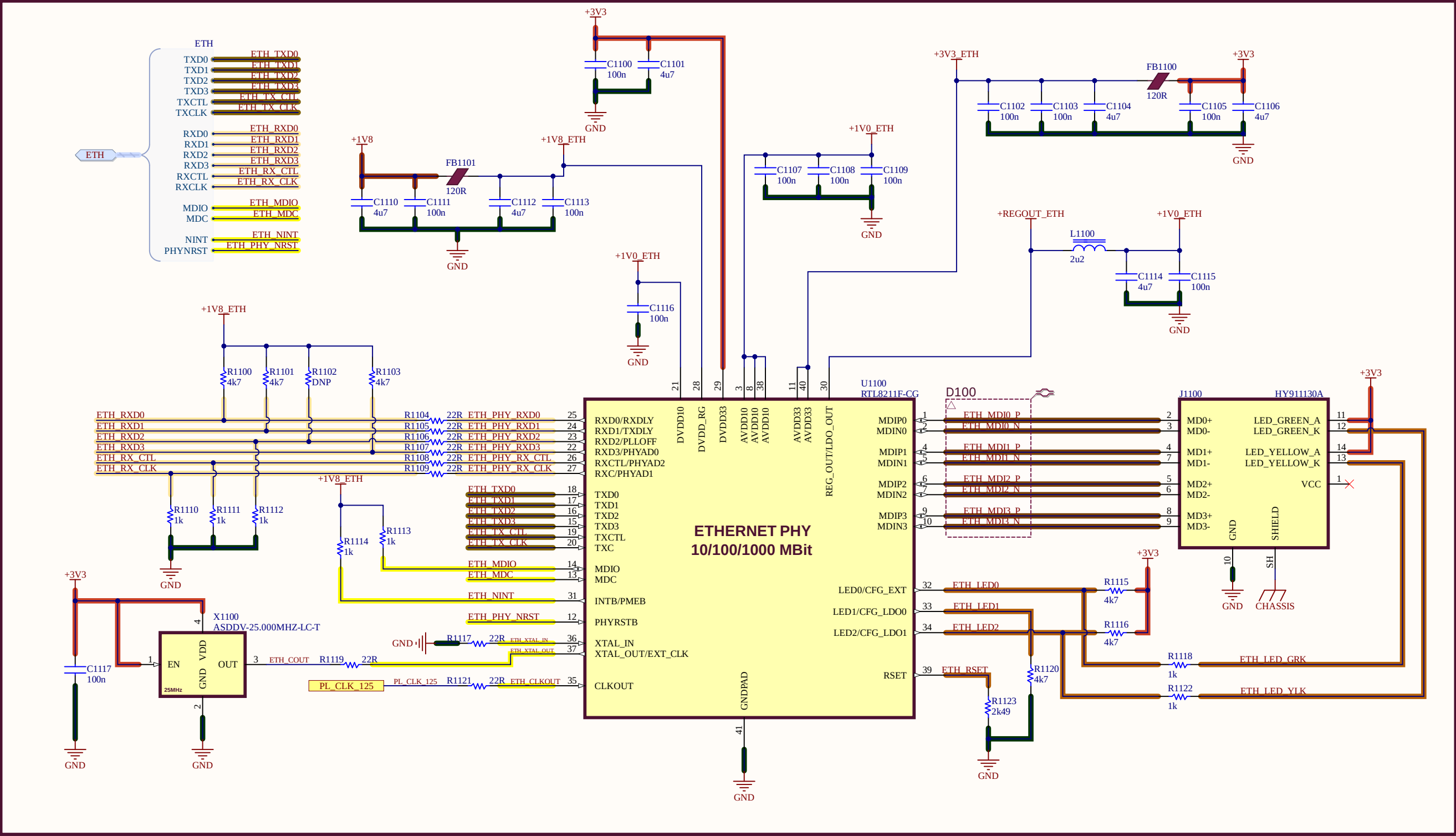
USB OTG PHY & Micro AB Connector



Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By		Sheet Name	
Uğur KELEŞ		ZHSD-USB-OTG.SchDoc	
Date	10.02.2026	Sheet	10 / 17
		Sheet Size A3	

ZHSD GIGABIT ETHERNET

Ethernet PHY & Magjack



Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By Uğur KELEŞ		Sheet Name ZHSD-ETHERNET.SchDoc	
Date	10.02.2026	Sheet	11 / 17
		Sheet Size A3	

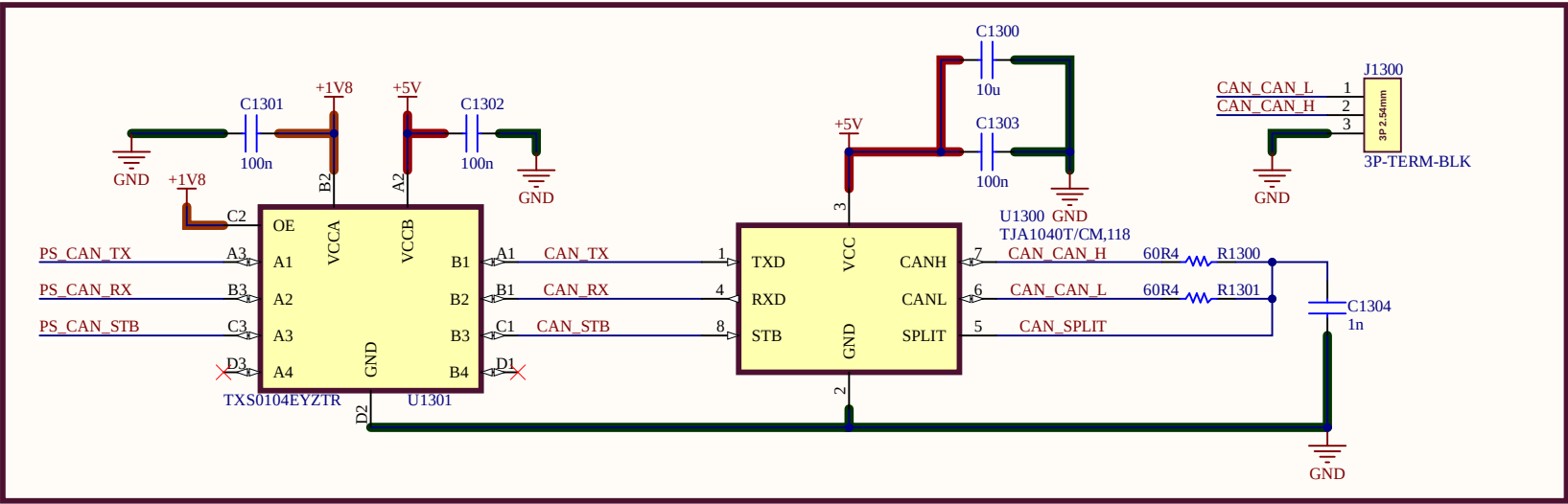
A

B

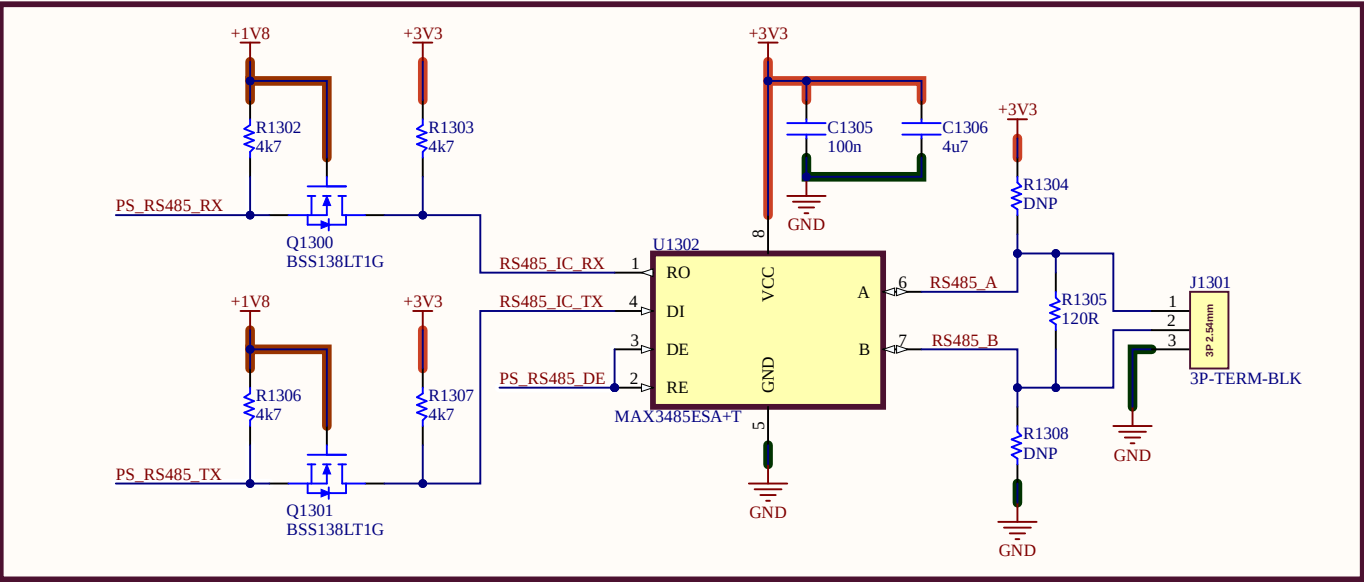
D

RS485 & CAN INTERFACES

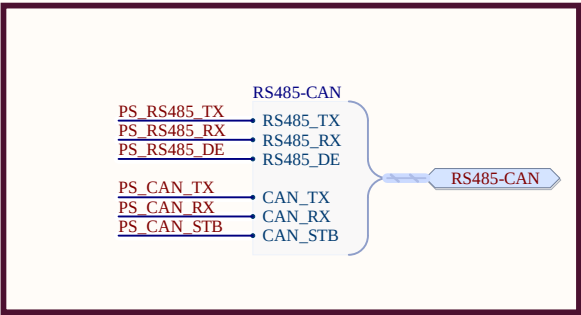
CAN Trceiver & Level Translation



RS485 Transceiver



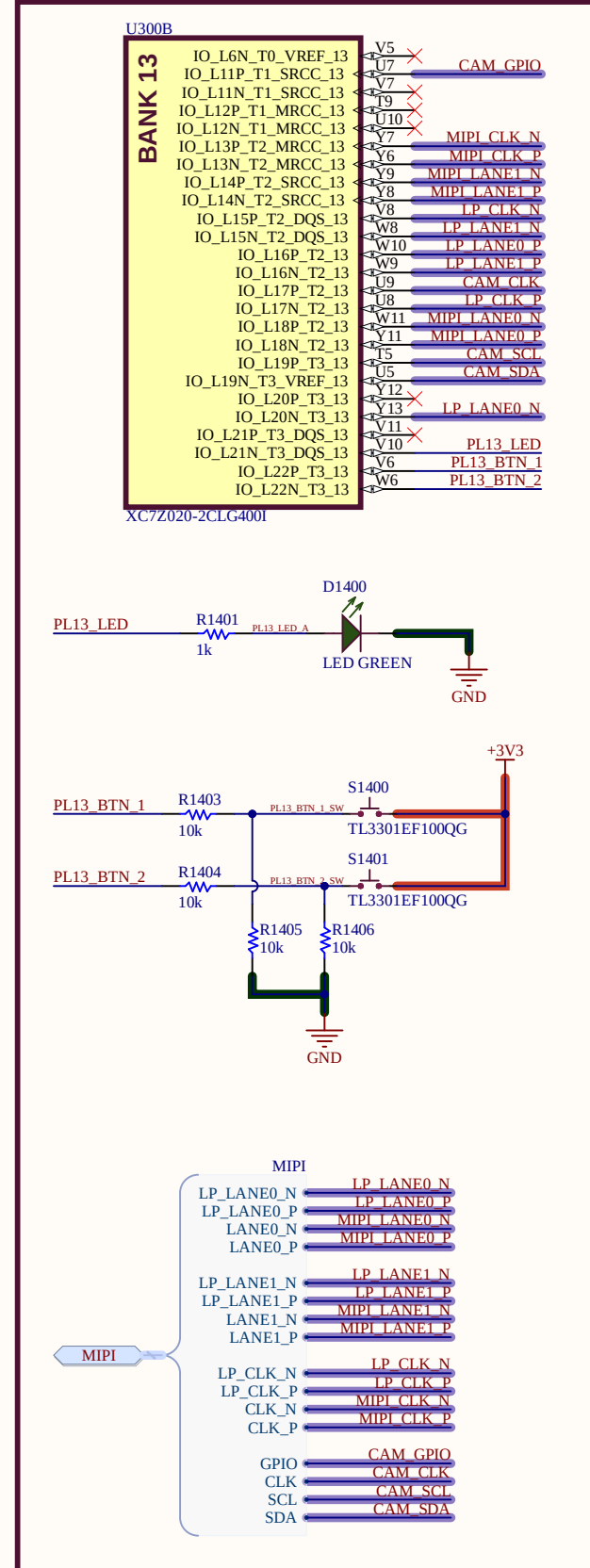
RS485 & CAN Harness



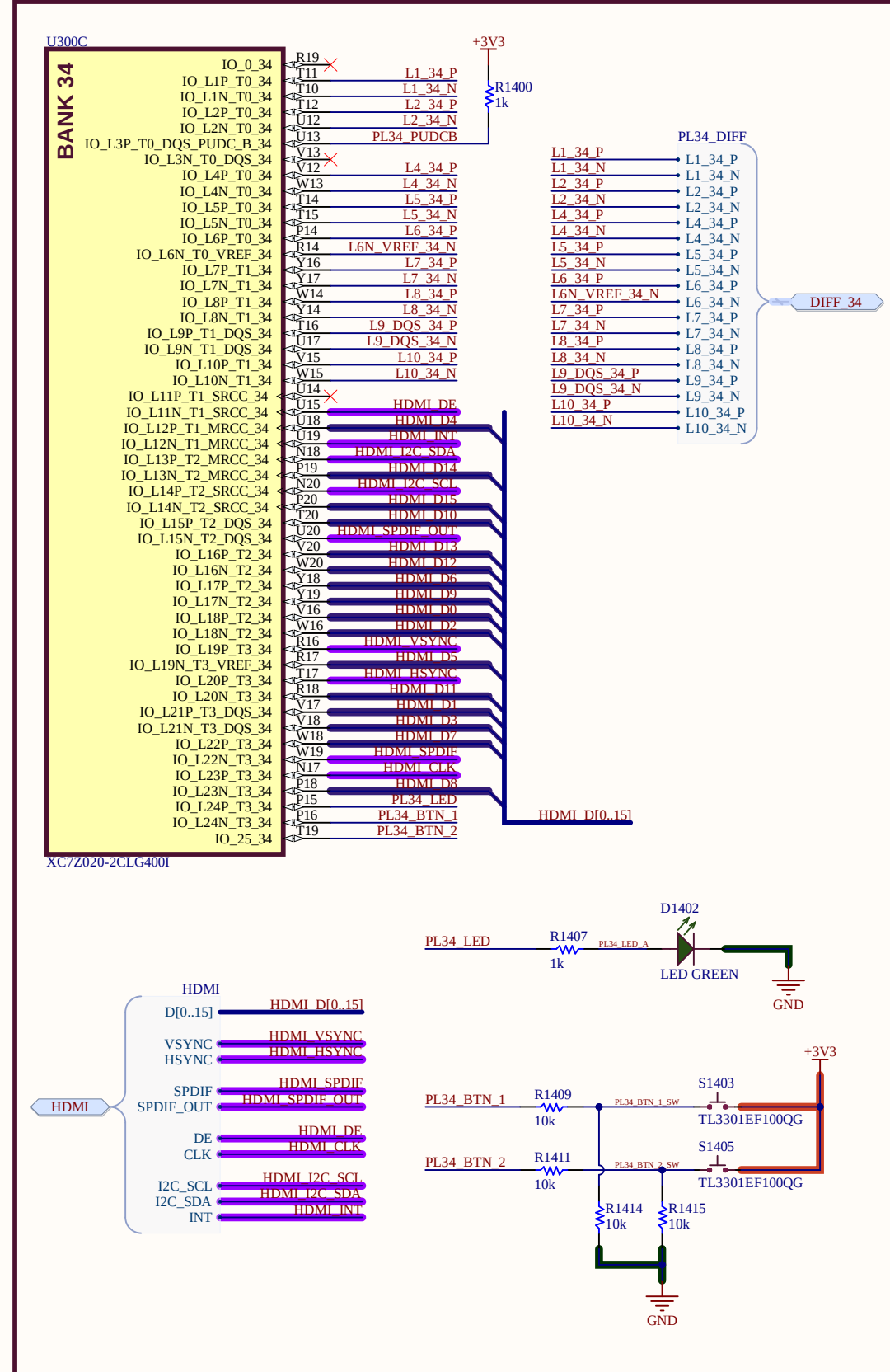
Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By		Sheet Name	
Uğur KELEŞ		ZHSD-RS485-CAN.SchDoc	
Date	8.02.2026	Sheet	13 / 17
		Sheet Size A4	

ZHSD ZYNQ PL BANKS

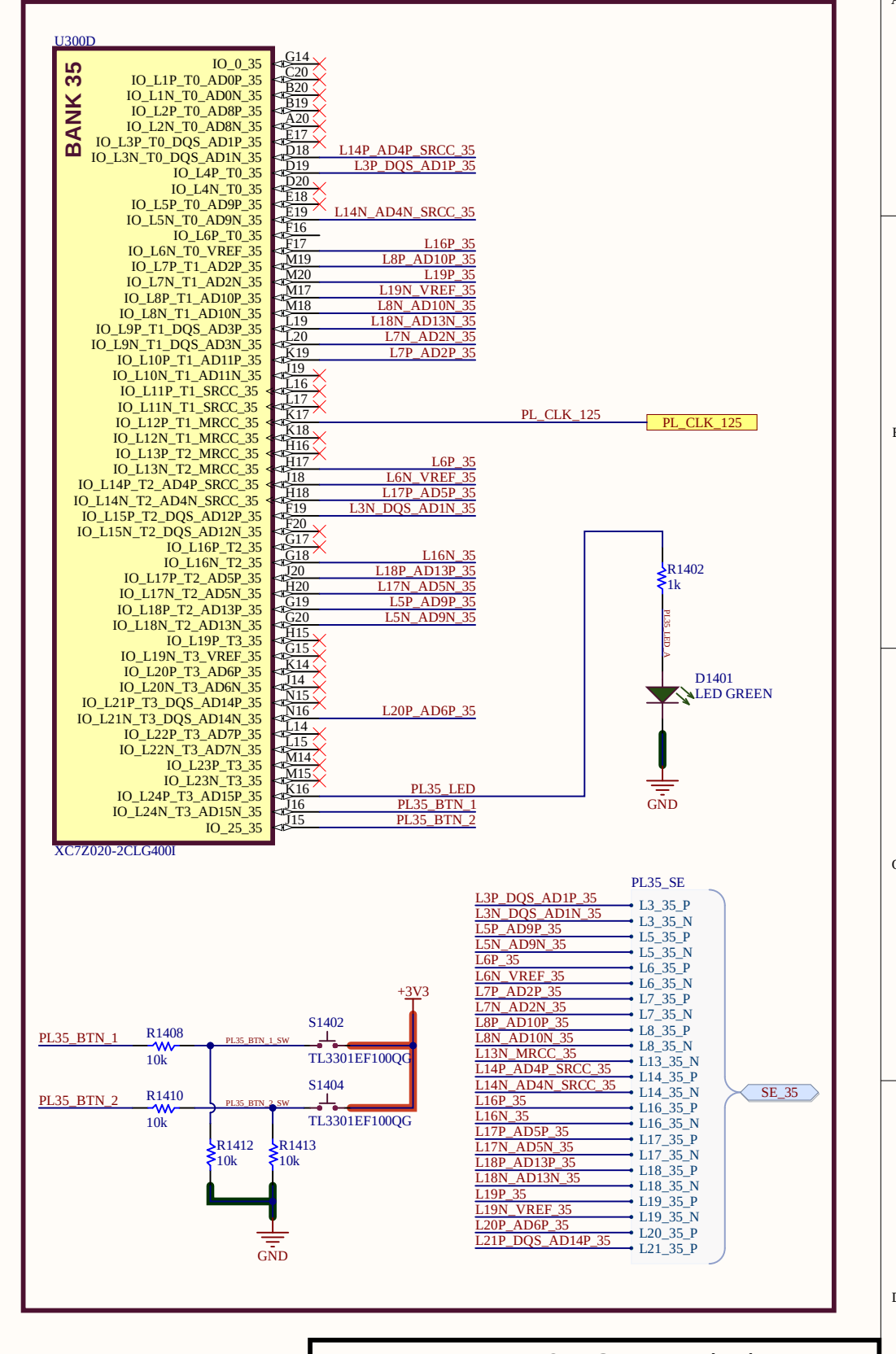
ZYNQ-7000 PL Bank 13 & MIPI Harness



ZYNQ-7000 PL Bank 34 & HDMI Harness



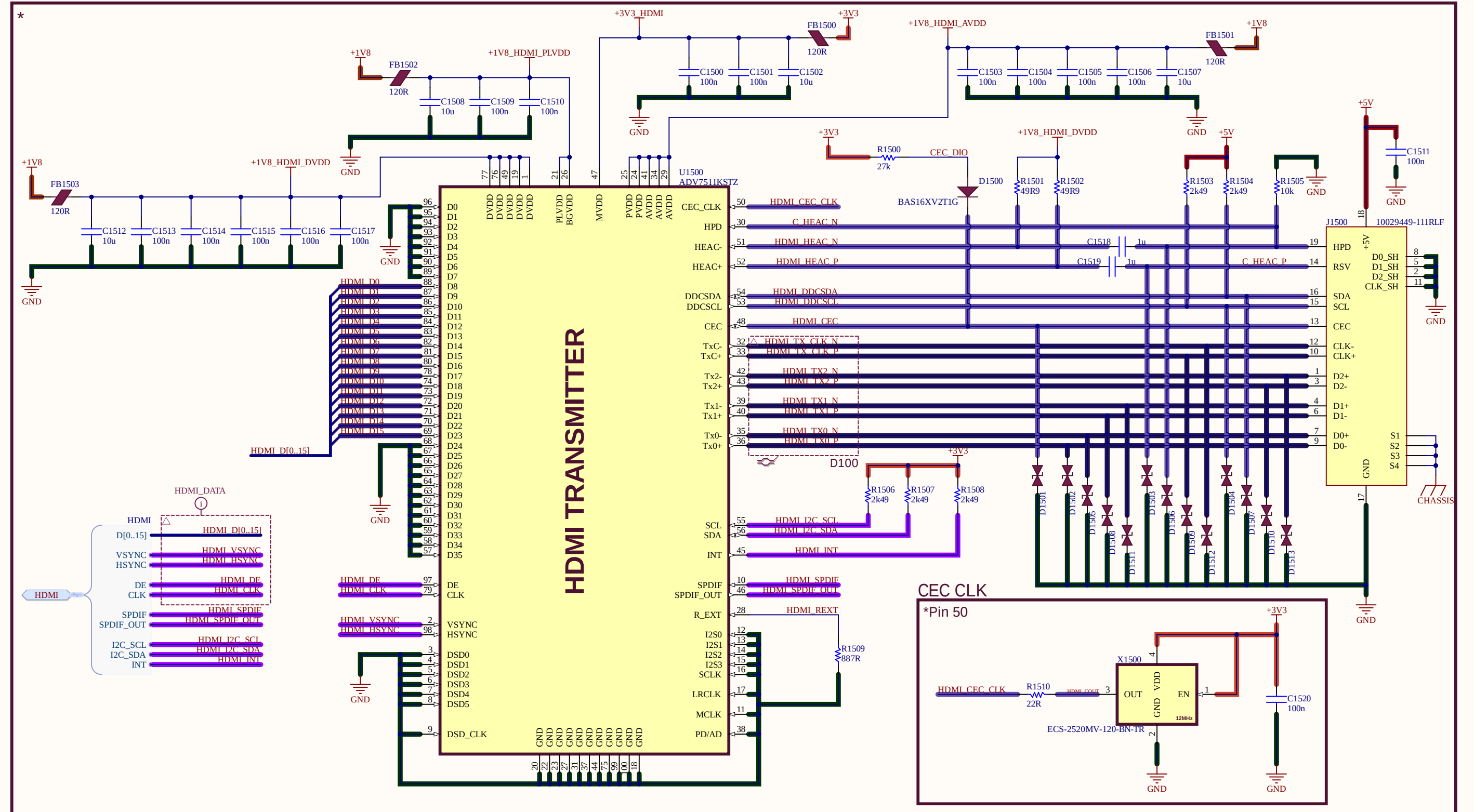
ZYNQ-7000 PL Bank 35



Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By		Sheet Name	
Uğur KELEŞ		ZHSD-ZYNQ-PL.SchDoc	
Date	11.02.2026	Sheet	14 / 17
		Sheet Size A3	

ZHSD HDMI INTERFACE

HDMI Transmitter and Connector

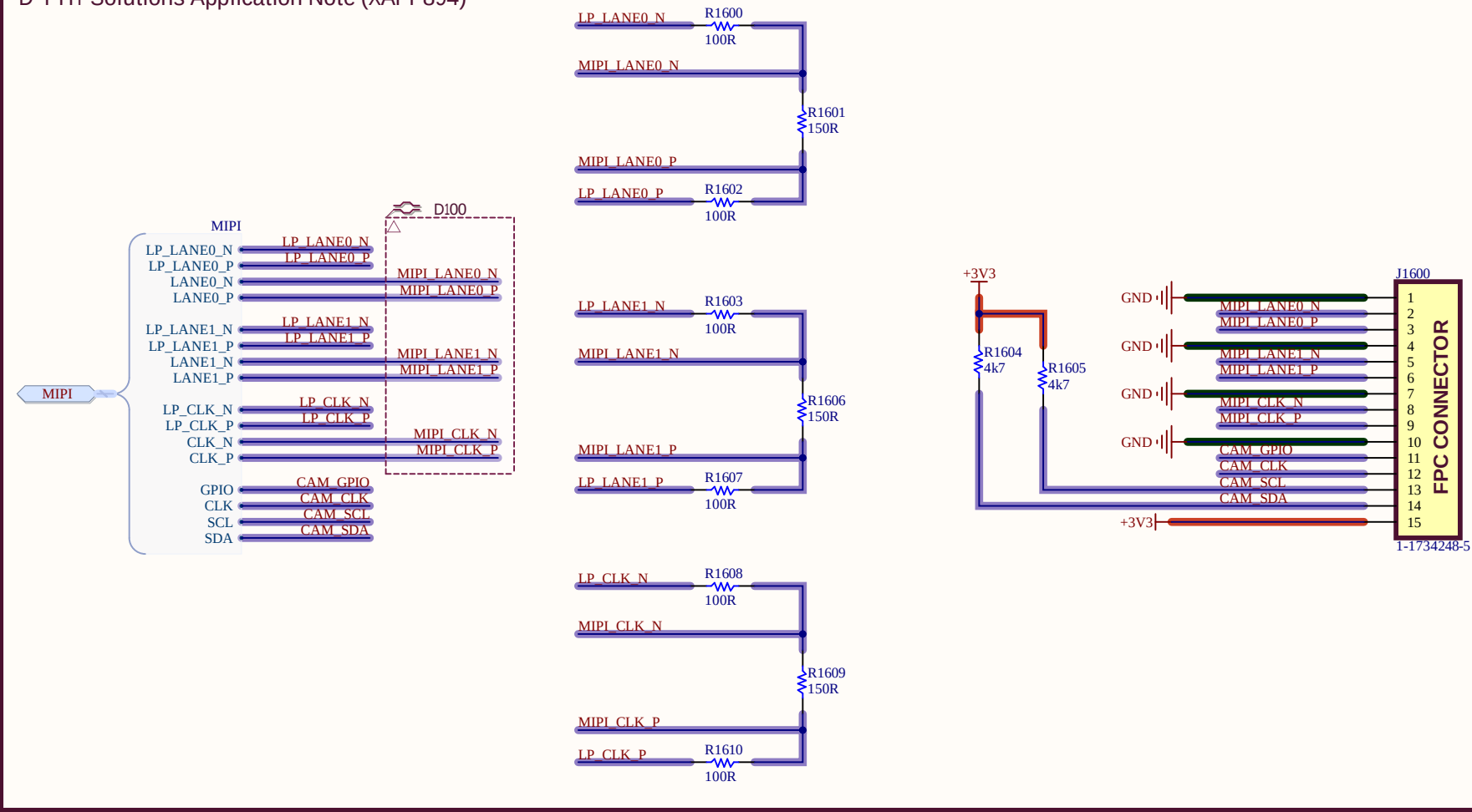


Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By		Sheet Name	
Uğur KELEŞ		ZHSD-HDMI.SchDoc	
Date	8.02.2026	Sheet	15 / 17
		Sheet Size A3	

ZHSD MIPI INTERFACE

MIPI CSI-2

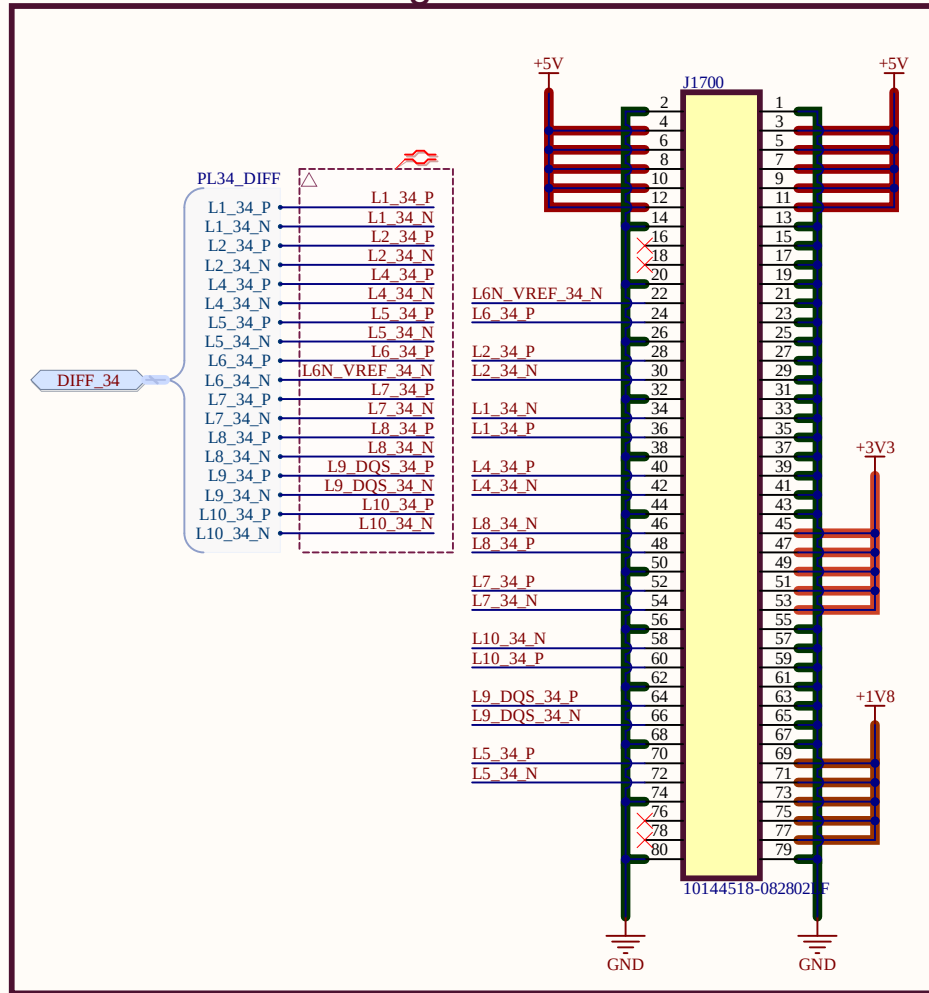
*D-PHY Solutions Application Note (XAPP894)



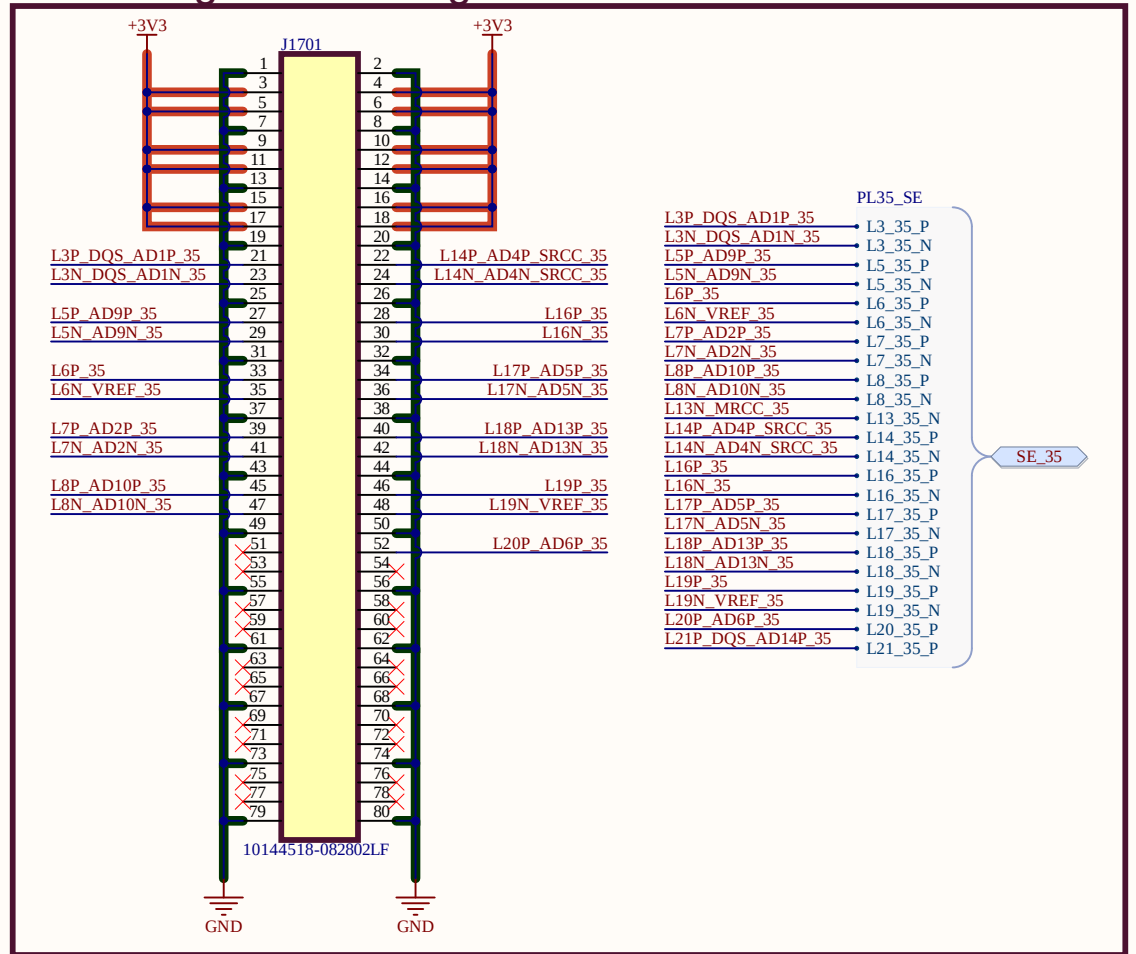
Project Title		ZYNQ-HS-DEV.PrjPcb	
Drawn By		Sheet Name	
Uğur KELEŞ		ZHSD-MIPI-CSI2.SchDoc	
Date	7.02.2026	Sheet	16 / 17
		Sheet Size A4	

ZHSD PL CONNECTIONS

PL34 Differential Signals



PL35 Single Ended Signals



Project Title ZYNQ-HS-DEV.PrjPcb

Drawn By
Uğur KELEŞ

Sheet Name
ZHSD-PL-CONNS.SchDoc

Date 9.02.2026

Sheet 17 / 17

Sheet Size A4

